Amendment to Claims

This listing of Claims will replace all prior versions and listings of claims in this Application.

Listing of Claims

Claim 1. (CURRENTLY AMENDED) A RRAM memory cell formed on a silicon substrate having a operative junction formed therein and a metal plug formed thereon on the operative junction, comprising:

a stack of the following layers, wherein each layer has the same horizontally disposed size as an immediately underlying layer:

a first oxidation resistive layer formed on the metal plug;

a first refractory metal layer formed on the oxidation resistive layer;

a CMR layer formed on the first refractory metal layer;

a second refractory metal layer formed on the CMR layer; and

a second oxidation resistive layer formed on the second refractory metal layer;

wherein "on" means directly on without any intervening structures.

Claim 2. (ORIGINAL) The RRAM memory cell of claim 1 wherein the oxidation resistive layers are formed of a material taken from the group of materials consisting of TiN, TaN, $TiAlN_x$, $TaAlN_x$, TaSiN, TiSiN, and RuTiN.

Claim 3. (ORIGINAL) The RRAM memory cell of claim 2 wherein the oxidation resistive layers have a thickness of between about 50 nm to 300 nm.

Claim 4. (ORIGINAL) The RRAM memory cell of claim 1 wherein the refractory metal layers are formed of a material taken from the group of materials consisting of Pt, Ir, IrO_2, Ru, RuO_2, Au, Ag, Rh, Pd, Ni, and Co.

Claim 5. (ORIGINAL) The RRAM memory cell of claim 4 wherein the refractory metal layers have a thickness of between about 3 nm to 50 nm.

Claim 6. (ORIGINAL) The RRAM memory cell of claim 1 wherein the CMR layer is formed of a material taken from the group of material consisting of CMR materials and high-temperature superconductors.

Claim 7. (ORIGINAL) The RRAM memory cell of claim 6 wherein the CMR layer has a thickness of between about 50 nm to 300 nm.

Claim 8. (ORIGINAL) A method of fabricating a multi-layer electrode RRAM memory cell comprising:

preparing a silicon substrate;

forming a junction in the substrate taken from the group of junctions consisting of N+ junctions and P+ junctions;

depositing a metal plug on the junction;

depositing a first oxidation resistant layer on the metal plug;

depositing a first refractory metal layer on the first oxidation resistant layer;

depositing a CMR layer on the first refractory metal layer;

depositing a second refractory metal layer on the CMR layer;

depositing a second oxidation resistant layer on the second refractory metal layer; and

completing the RRAM memory cell.

Claim 9. (ORIGINAL) The method of claim 8 wherein said depositing the oxidation resistive layers includes depositing a material taken from the group of materials consisting of TiN, TaN, $TiAlN_x$, $TaAlN_x$, TaSiN, TiSiN, and RuTiN.

Claim 10. (ORIGINAL) The method of claim 9 wherein said depositing the oxidation resistive layers includes depositing the oxidation resistive layers to a thickness of between about 50 nm to 300 nm.

Claim 11. (ORIGINAL) The method of claim 8 wherein said depositing the refractory metal layers includes depositing a material taken from the group of materials consisting of Pt, Ir, IrO_2, Ru, RuO_2, Au, Ag, Rh, Pd, Ni, and Co.

Claim 12. (ORIGINAL) The method of claim 11 wherein said depositing the refractory metal layers includes depositing the refractory metal to a thickness of between about 3 nm to 50 nm.

Claim 13. (ORIGINAL). The method of claim 8 wherein said depositing a CMR layer includes depositing a layer of CMR material taken from the group of material consisting of PCMO, LPCMO and high-temperature superconductors.

Claim 14. (ORIGINAL) The method of 13 wherein said depositing a CMR layer includes depositing a layer of CMR material having a thickness of between about 50 nm to 300 nm.